CLAIMS

What is claimed is:

1. A method of making a semiconductor device, comprising:
providing a substrate having a semiconductor layer over a first insulating layer;
forming a second insulating layer on the semiconductor layer having a thickness not greater than about 100 Angstroms;
forming an anti-reflective coating (ARC) on the second insulating layer;
etching an opening through the ARC, the second insulating layer, and the semiconductor layer, and into the first insulating layer;
forming a third insulating layer along a sidewall of the opening;
filling the opening with dielectric fill material;
removing the ARC and the second insulating layer;
forming a gate dielectric;
forming a conductive layer on the gate dielectric; and
patterning the conductive layer.

2. The method of claim 1, wherein the filling the opening comprises depositing oxide by high density plasma.

3. The method of claim 1, wherein the forming the third insulating layer comprises growing oxide.

4. The method of claim 1, further comprising applying a wet etch prior to forming the third insulating layer and after forming the opening.

5. The method of claim 1, wherein the conductive layer is polysilicon.

6. The method of claim 1, wherein the conductive layer further comprises silicide.

7. The method of claim 1, wherein the second insulating layer has a thickness of not greater than 100 Angstroms.

8. A method of preparing a semiconductor device for formation of a gate, comprising:
providing a semiconductor substrate having a semiconductor layer over a first insulating layer;
forming a second insulating layer on the semiconductor layer;
etching an opening through the second insulating layer, and the semiconductor layer, and into the first insulating layer to expose a surface of the first insulating layer;
forming a third insulating layer along a sidewall of the opening without forming a void between the third insulating layer and the surface of the first insulating layer; and
filling the opening with dielectric fill material.

9. The method of claim 8, further comprising.
forming a fourth insulating layer over the second insulating layer prior to forming the third insulating layer; and
performing an isotropic etch prior to forming the fourth insulating layer to cause a recess in the second insulating layer;
wherein
the forming the third insulating layer avoids formation of an undercut region in the second insulating layer.

10. The method of claim 8, wherein the second insulating layer has a thickness that is not greater than about 100 Angstroms.

11. The method of claim 8, wherein the third insulating layer is not greater than 50 Angstroms.

12. The method of claim 8, further comprising:
removing the second insulating layer; and
forming a gate dielectric on the semiconductor layer.

13. A method of preparing a semiconductor device for formation of a gate, comprising:
providing a semiconductor substrate having a semiconductor layer over a first insulating layer;
forming a second insulating layer on the semiconductor layer;
forming a third insulating layer on the second insulating layer;
etching an opening through the second insulating layer, the third insulating layer and the semiconductor layer, and into the first insulating layer;
performing an isotropic etch to cause a recess in the second insulating layer;
forming a fourth insulating layer along a sidewall of the opening without leaving a recess between the second insulating layer and the third insulating layer; and
filling the opening with dielectric fill material.

14. The method of claim 13, wherein filling the opening comprises depositing an oxide using high density plasma.

15. The method of claim 13, wherein the second insulating layer is not greater than 100 Angstroms.

16. The method of claim 13, wherein the fourth insulating layer has a thickness that is not greater than 50 Angstroms.

17. The method of claim 13, wherein:
the etching of the opening exposes a surface of the first insulating layer; and
the forming the fourth insulating layer avoids forming a recess between the fourth insulating layer and the surface of the first insulating layer.

18. A method of making a semiconductor device, comprising:
providing a substrate having a semiconductor layer over a first insulating layer;
forming a second insulating layer on the semiconductor layer;
forming an anti-reflective coating (ARC) on the second insulating layer;
etching an opening through ARC, the second insulating layer, and the semiconductor layer, and into the first insulating layer;
forming a third insulating layer along a sidewall of the opening having a width not greater than 50 Angstroms;

filling the opening with dielectric fill material;
removing the ARC and the second insulating layer;
forming a gate dielectric;
forming a conductive layer on the gate dielectric; and
patterning the conductive layer.

19. The method of claim 18 wherein the second insulating layer has a thickness not greater than 100 Angstroms.

20. The method of claim 18, wherein filling the opening comprises depositing oxide by high density plasma.

21. The method of claim 18, wherein the forming the third insulating layer comprises growing oxide.

22. The method of claim 18, further comprising performing an isotropic etch prior to forming the third insulating layer and after forming the opening.

23. The method of claim 18, wherein the conductive layer is polysilicon.

24. The method of claim 23, wherein the conductive layer further comprises silicide.

25. The method of claim 18, wherein the etching the opening is further characterized as etching no more than 50 Angstroms into the first insulating layer.